HIGH EFFICIENCY 4 GHz SSPA FOR SPACE APPLICATION

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ABSTRACT

A high efficiency 4 Ghz SSPA has been developed for on-board satellite application. The amplifier utilizes state-of-the-art internally matched devices that allow good performances and reduced alignment time. The obtained results make the substitution of the traditional TWTA highly convenient, in terms of reduced weight, increased reliability and improved RF performance.

INTRODUCTION

In the last few years the design and manufacturing technology of high-power GaAs FET devices, operating at C-band, has improved to the point that reliable, high performing devices are presently available on the market. The present and next generation of 6/4 GHz transponders for satellite applications has taken advantage of this situation for the substitution of the traditional TWT amplifier with Solid State Power Amplifiers. This substitution is convenient in terms of:

- higher reliability
- weight reduction
- better electrical performance
- increased flexibility

The higher reliability is due to the use of semiconductor devices that do not present phenomena like cathode wear-out (TWTA) and other recognized failure modes associated with high voltage operation(TWTA and Electronic Power Conditioner for TWTA). The weight reduction is due to the reduced complexity of the EPC (elimination of high-voltage biasing) and the less bulky housing of the SSPA. In addition a larger weight reduction can be obtained by utilizing a centralized EPC that supplies more than one power amplifier. This last capability is not feasible for TWTAs due to the very high biasing voltages.

The better electrical performance can be summarized in terms of wider bandwidth, lower noise-figure, but especially higher linearity. This characteristic allows the use of the power amplifier closer to saturation, increasing the channel capability and utilizing more efficiently the on-board power.

An SSPA is also more flexible than a TWTA: different system or customer requirements (different gain settings, AGC, commandable gain, temperature compensation, power monitor, etc.) can be satisfied simply by changing the number of amplifying modules or adding into the line-up additional modules such as variable-attenuators or detectors.

SSPA GENERAL DESCRIPTION

The amplifier block diagram is shown in Fig.1. The operating bandwidth of the modules decreases, going from the input to the ouput, to improve the power and efficiency performance and, at the same time, minimize the retuning for operation over the different transponder channels. The gain compensation of the amplifier over the temperature range is obtained with a dedicated pin-diode attenuator. This allows a simple adjustment, a reduction of the number of tests at module level and a simplification of the FET biasing circuits. The pin-attenuator is controlled by a resistive network containing a thermistor. The resistor values are optimized (using an in-house program) to change the attenuation of the module over the temperature range in a suitable fashion to compensate the variation of all the SSPA modules. A suitable overload circuit is inserted to protect excessive power from being applied to the interstage, driver and output stage during an input overload. The circuit consists of a detector, a pin-diode variable attenuator and a dc control circuit. The modules of the overload circuit can be reconfigured in a different line-up to perform operations like: AGC, commandable gain and power monitor. Internally matched devices are used at the output to simplify the alignment procedures. In addition, the devices have been chosen to be able to deliver the rated output power using only two devices. This improves the manufacturability and reduces the overall dimensions of the unit. All the modules have been implemented utilizing microstrip structures on alumina substrates or ferrite substrates (for the isolators). The substrates and the FET devices are then soldered on kovac carriers that can be easily tuned separately and then integrated into the unit chassis. For the power stages, the FET devices

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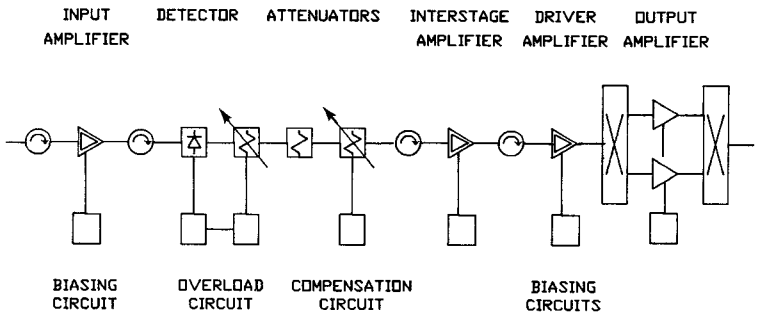

Figure 1 - SSPA Block Diagram

are directly soldered to the housing to reduce the thermal resistance from the channel to the external environment.

SSPA MODULE DESCRIPTIONS

The input amplifier is a two stage amplifier utilizing low-noise NE673-83 devices connected by three alumina substrates on which matching and biasing elements are implemented utilizing microstrip and discrete components. The amplifier has been designed to provide high gain and low noise figure and to be unconditionally stable over the frequency range 2 to 18 GHz. The detector utilizes a 15 dB coupler and a matched pair of schottky diodes. One diode detects the power flowing along the line and the other compensates the detected voltage over the operating temperature range.
The Pin-diode variable attenuator utilizes two 3 dB couplers and two pin diodes connected in a balanced configuration in order to operate over a wide frequency range and provide soft degradation in case of the failure of one diode. Two identical modules are connected in cascade with a fixed attenuator to perform the following operations: gain compensation over temperature, overload protection and adjusting of the nominal gain value during the amplifier alignment.
The ferrite isolators provide decoupling between the adjacent stages as well as good matching at the SSPA input port.
The interstage amplifier provides a medium power amplification of the signal and utilizes a NE 673-83 device in cascade with a NE 9001-75 device. The amplifier has been designed to operate over a wide frequency range, to be unconditionally stable over the frequency range 2 to 18 GHz and deliver enough power to drive the following stages.
The driver amplifier amplifies the signal to a level that drives the output devices at an optimum efficiency point. This has been achieved with an optimum choice of the devices and of the biasing point. The utilized devices are the Ne 8002-96 and FLC 30ME. The amplifier has been designed to provide maximum output power keeping the gain to a reasonable value over a wide bandwidth. The operating point has been chosen to maximize the output power capability and the efficiency.
The output amplifier represents the most critical part of all the design. For this reason particular attention has been dedicated to the evaluation of different power devices and the choice has been made considering the following factors: efficiency, low thermal resistance and reliability. Two devices have been identified: the Avantek IM-3742/6 and the Fujitsu FLM 3742-8B. Both or them are internally matched and have electrical characteristics such that a design utilizing only two devices connected in parallel by 3 dB hybrid couplers gives a performance better than initial specifications.
Particular care has been also devoted to the design of the 3 dB hybrids in order to reduce to a minimum the insertion loss and the imbalance. The selected structure has been a 3 dB, 90 deg. Lange coupler implemented on 50 mil alumina substrate to minimize the conductor loss. In order to ensure good repetibility the couplers are etched using the ion-beam milling technology.
The performance of the output amplifier are reported in table 1. The output power can be adjusted by changing the biasing of the devices with minimum impact on the other performances. Even if the devices used in the output amplifier are able to operate over the full frequency range 3.7 to 4.2 GHz, the operating bandwidth is reduced during the amplifier alignment in order to improve its efficiency, as shown in fig. 2.

TEST RESULTS

The output amplifier has been tuned over the frequency range 4.140 to 4.200 Ghz, which represents in terms of power capability and efficiency the worst case channel over the bandwidth 3.7-4.2 GHz. The integrated unit has been tested over an extended temperature range of -35 to +70 C and the measured performances are reported in table 1. The output power/efficiency versus input power curves are shown in fig. 3

TABLE I

Gain at rated power	9 dB
Freq. Range any 60 MHz over 3.7 to 4.2 GHz	
Rated power	12 W
Efficiency at rated power	48%

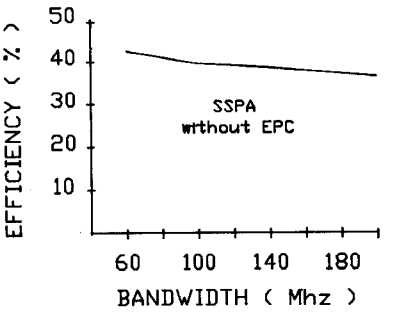

Figure 2 - SSPA Efficiency vs Bandwidth

SYSTEM IMPROVEMENTS

The obtained efficiency is extremely high and very close to that of a high performing TWTA (45%). Therefore, considering the operation at the saturation point, even though a TWTA would require a smaller and lighter solar array, the reduction of weight obtainable with a SSPA becomes highly attractive.
Curve A of figure 4 illustrates this concept, by showing the typical weight of a 24 channel transponder versus efficiency of the power amplifier for a HS-393 satellite bus. The crossing point where a SSPA is more convenient in terms of weight is at an efficiency value of 37%. With the obtained results the weight reduction would be 25 Kg. Curve A has been plotted considering a dedicated EPC for each power amplifier. If a centralized EPC is used, the advantage of using SSPAs becomes even higher and the crossing point decreases to 35%. With the developed SSPA this would mean a reduction of 44 Kg. of the transponder weight.
The linearity improvement is shown in fig. 5 where the third order C/I for a two carrier signal in a TWTA and in the designed unit are compared. Even if the two types of power amplifiers give similar performance close to saturation, the SSPA becomes clearly better in the back-off mode. For a link requirement of 25 dB C/I the TWTA has to be operated at 14 dB IBO (input back-off) where its efficiency is 13% whereas this SSPA will work at 10 dB IBO with an efficiency of 17%. Also in terms of reliability the SSPA is far better than the traditional TWTA. Fig. 6 shows the SSPA fit count versus operating base plate and has to be compared with a TWT whose failure rate can be approximated by 1000 fits. If the comparison is made at transponder level the probability of mission success at the satellite end of life (12 years), for a 24 channel transponder using 30 SSPAs with centralized EPC is 37% better than that of the same transponder, using 30 TWTAs and individual EPCs.

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TABLE II

	-5/+55 C	-35/+70 C
Operating frequency range (GHz)	4.140-4.200	4.140-4.200
Rated output power (W)	11.9	11.5
Gain @ rated power (dB)	57.8	57.4
Gain variation over 36 MHz @ rated power (dB)	0.2	0.2
Gain stability over temperature (dBpp)	0.5	0.8
Group delay over 36 MHz (nS)	0.5	0.5
AM/PM up to 10 dB IBO (deg/dB)	2.8	3.8
Harmonics at output (dBc)	25	25
Efficiency at rated output (%)	44	43
Overdrive 20 dB above input rated level	no damage	no damage
Noise Figure (dB)		
nominal operation	2.9	3.1
overload	3.9	4.1
Weight	770 g.	

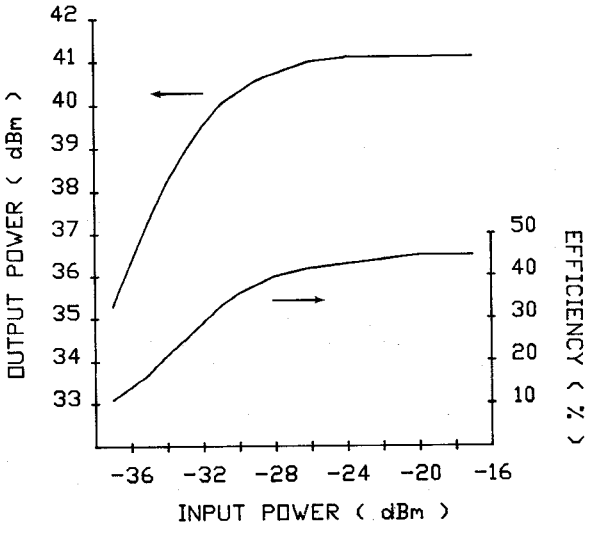

Figure 3 - Pout and Efficiency vs PIN

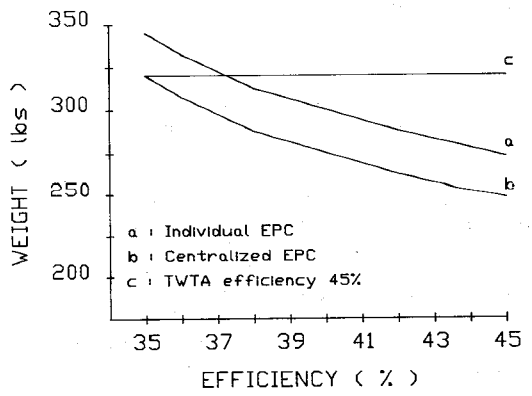

Figure 4 - Weight vs/Efficiency

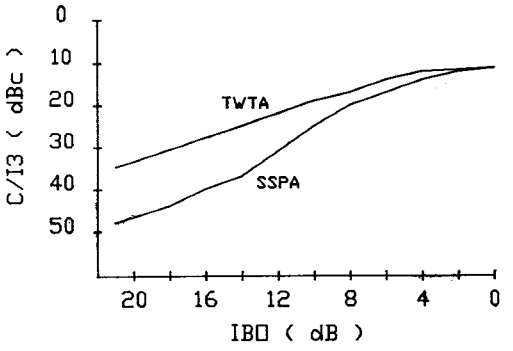

Figure 5a - Intermodulation vs Input Backoff

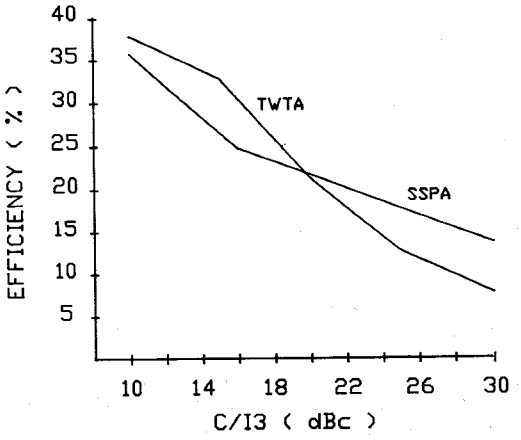

Figure 5b - Efficiency vs Intermodulation

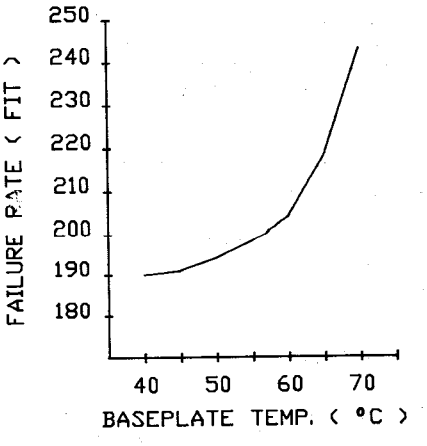

Figure 6 - SSPA Failure Rate